Imperial College
London

Lecturer Name: Professor Peter Cheung (1081)

Survey Name: SOLE UG Autumn 2017

Digital Electronics 2 (EE2-01)

Individual Lecturer Feedback (Professor Peter Cheung)

1) The lecturer explained the material well					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
46	14	2	1		

2) The lecturer generated interest and enthusiasm					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
55	7	1			

3) The lecturer was approachable					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
55	8				

4) Overall, I am satisfied with this lecturer					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
52	8	1			2

The following free text comments were received:

5) Please use this box to provide any additional constructive feedback to this lecturer:

- A great lecturer with strong enthusiasm for whatever he is teaching. I have enjoyed our brief conversations in and out the lab. Thank you again
- Excellent Lecturer showed experience is everything when lecturing, pace was perfect and the lecturer identified the points that students couldnt understand perfectly. Lecture was almost perfect in its structure and sync to the experiment with the exception of part 4 which was a week in delay however the module content was both interesting and intelectually stimulated and refined to perfection. Especially liked the format of the problem classes which should be reiterated to other lectures as it kept students engaged and provided real time feedback on what we understood,
- Had great notes with detailed explanation. For concepts covered in first year spend less time on them. Instead of giving equal weighting to things recapped from first year and new material brought.
- Professor Cheung clearly loves teaching, especially this module.
- Coordination of lectures, labs and maintaining course website was excellent.
- Your enthusiasm makes the lectures and thus the module much more enjoyable.
- Sometimes it is a little bit hard to follow what is going on the slide during the lecture. It takes some time to work out what the purpose of the slide is. The lecturer could do better in repeating things and continously explaining the context. During some lectures I didn't understand one slide, rendering all consequent slides meaningless to me.
- Peter Cheung is a brilliant lecturer who really is enthusiastic about the subject which really rubs off on us!
- I love the way he teaches. Very interesting and relevant to the labs.
- Very interactive module and the problem class are very helpful to fully understand.
- good sense of humour and course material well tied with the experiment
- sometimes, I could not understand what the lecturer mean, his explanation was vague and not very clear. but the explanation on the handouts was much better.
- Speed up during lecture.
- Exceptional and very knowledgeable lecturer. Definitely valuable to the department.
- Great teacher. Clearly enthusiastic about the subject
- Prof. Cheung's dedication and approach to the course, especially the labs, has been exemplary. Thank you very much.
- The content was definitely delivered at the right pace, and the amount of the explanation provided to explaining certain principles was just right. The lecturer is very student friendly and approachable, and I am very happy to ask him questions related to his experiment and to his lecture course

Immediately below are the collated numerical results received for the Module.

Module Feedback - Digital Electronics 2 (EE2-01)

1) The content of the module is well structured					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
36	22	2	1	1	1

2) The content of the module is intellectually stimulating					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
36	22	3	1		1

3) Where applicable, I have received helpful feedback on my work submitted so far					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
21	19	4	2	1	16

4) Overall, I am satisfied with the quality of the module					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
34	24	3	1		1

The following free text comments were received:

5) Please use this box to provide any additional constructive feedback on this module. Students with a disability are invited to make specific suggestions for improvement that would assist them:

- Links fantastically with the lab experiment.
- Feels like this course just taught Verilog. Needs to introduce more digital circuits, like how ADC and DAC were introduced. Less of FSM counters etc, already learned how they work in first year.
- the lab is "veri" interesting but having the oral in the last week, is really bad(for EIE)
- My only wish is that the first few slides of this module could have been provided in advance of the EIE year one project to explain how FPGA's actually work
- The link between module and experiment was excellent and provided stimulus for engagement as students directly saw and implemented the link of the knowledge acquired to real life tasks. This also provided valuable feedback on what we have learnt so far. This should be replicated in all modules and their respective experiments where possible! Only comment to be made is the one week delay in said knowledge to the labs however most of the time the lectures and experiment ran in parallel excellent module!
- It is great that the course is intertwined with the lab Verilog session. We are able to apply concepts in the lab and likewise lab analysis in the written module. All I'd say is to perhaps re-arrange some lecture orderings. For example, lecture 16, which clarified the last section of the lab session was given a day after the first groups lab session on Monday morning. Why not put that the week before and then do lecture 15 in the last week. Spent a lot of time trying to work things out that morning, which were actually in lec 16 if I had knew about it.
- It would be nicer if I received higher marks on the FPGA oral exam!
- 1) Making us work in the Problem Classes is a definite positive: Perhaps reduce the number of "explain it" questions and give longer questions to solve.
  2) VERILOG lectures were very helpful but unfortunately they almost always were the Monday slot in the lab. Please restructure the lecture order to ensure everyone gets the lecture before their lab slot.
- Very interesting and relevant course. Most of the confusion people had with the course is that there are some major differences in Moore and Mealy Diagrams that were taught in digital electronics last year. Please could the two courses leaders get together and make the courses consistent with each other
- A fairly complex course at first, but very well guided throughout. Very well organised self-study component.
- I really enjoy the content being covered in digital electronics at the moment. There is plenty of practical application in the world of FPGAs. The sections are divided up quite nicely, and allows one to develop through to the more difficult content with ease. The tutorial classes are well strutted as well with full descripted answers to the questions
- Very good lecturer
- I extremely enjoyed the fact that the Lab was so closely connected to the lectures
- Lectures tie in very well with labs

  some syntax errors in notes and examples - GTAs very helpful in finding them though
- The synchronisation of the lab experiment and lectures is very helpful. The notes are exhaustive and all information is explained well. The structure of the problem classes is very nice, and more interactive than in any of the other modules!

  Perhaps compile all the lecture handouts into a single handout to be distributed at the beginning of the term, to make simultaneously using information provided in different lectures easier.
- The homework is rarely explained in time. The problem class often become lecture and homework is not explained fully.
- Interesting. Loved that it wasvin sync with the lab. Well done.
- I think we may have spent a bit too much time on the VERI experiment during lecture hours. Coloured notes would have been very helpful.
- Good module. The way it was integrated with the lab veri experiment was very good. All courses should be more integrated with the lab rather than feeling separate.

E2 Electronics Lab (EE2-LABE)

Individual Lecturer Feedback (Professor Peter Cheung)

1) The lecturer explained the material well					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
35	11				

2) The lecturer generated interest and enthusiasm					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
41	5				

3) The lecturer was approachable					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
41	5				

4) Overall, I am satisfied with this lecturer					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
38	7				1

The following free text comments were received:

5) Please use this box to provide any additional constructive feedback to this lecturer:

- As for my comments on the digital module - thank you
- Please see both feedback for lab content and digital module.
- Please give me higher marks on the FPGA oral!!!
- Really fantastic how Prof Cheung was in the lab for every single lab session to answer questions.
- Very good
- I think the VERI experiment was very interesting. However, I really do not think that completion of the "optional" bits should be part of the marking scheme.
- Enthusiastic and helpful
- The lecturer has a great involvement with the student cohort and uses what available time he has to help students with the experiment in whatever way he can. The content from the lectures has a direct link to the lab and everything is very well explained. The experiment is extremely well designed with almost no errors in it at all.
- Very time consuming experiment, only works if the other lab slot is free.

Immediately below are the collated numerical results received for the Module.

Module Feedback - E2 Electronics Lab (EE2-LABE)

EIE2 Electronics Lab (EE2-ILABE)

Individual Lecturer Feedback (Professor Peter Cheung)

1) The lecturer explained the material well					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
9	4				

2) The lecturer generated interest and enthusiasm					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
9	4				

3) The lecturer was approachable					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
10	3				

4) Overall, I am satisfied with this lecturer					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
10	3				

The following free text comments were received:

5) Please use this box to provide any additional constructive feedback to this lecturer:

- Too much content for available lab time
- Gave the best lab since startling at Imperial. Well laid out and planned. An improvement would be don't call some parts of the lab optional if in reality they are necessary for getting a 2:1 or above, by that logic about half the degree if optional. Optional implies that if you do it you won't gain any extra marks but is just to further persona knowledge and experience
- Excellent, as he is in lectures.

Immediately below are the collated numerical results received for the Module.

Module Feedback - EIE2 Electronics Lab (EE2-ILABE)

1) The content of the module is well structured					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
1	5	2	5		

2) The content of the module is intellectually stimulating					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
2	7	4			

3) Where applicable, I have received helpful feedback on my work submitted so far					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
4	3	2	3		1

4) Overall, I am satisfied with the quality of the module					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
2	4	2	3	2	

The following free text comments were received:

5) Please use this box to provide any additional constructive feedback on this module. Students with a disability are invited to make specific suggestions for improvement that would assist them:

- Poorly designed to go through large expanses of material rather than focus on actual learning. Pairing was ineffective and left a lot of individuals alone for no apparent reason. Definitely not enough time within allocated time slots to finish the labs. A lot of delays comes with the learning environment rather than the actual syllabus. Some UTAs extremely helpful. Others not so much
- Electronic labs seem mostly pointless, specifically the first lab on DFT which really didn't tie in to any modules being studied at the time. The second lab on Verilog is much more relevant and better structured.
- DFT: Inconsistent feedback from UTA an GTA. Some said to skips certain parts yet they were discussed in the oral. No indication of whether what the students are doing is correct or not.
- DFT work was dull. VERI Lab has been ok so far, although there is too much content expected of you.
- The lab content is good, however too much material to cover in the available lab time we have. Also accounts for such a large % of our year when say our MIPS simulator requires much more work and count for a lot less than one lab.
- VERI is the best lab so far
  DFT is really bad. There should be at least a 1hour session on MATLAB before you start the lab. The worst thing is that being at the beginning of the term it involves concepts that are introduced later in the lecture.
  A solution would be to have 2 sessions per week and push the labs later in the term
- Labs are mind numbing. If there is someway to make 3 hours of sitting in front of computer and oscilloscope more stimulating then should try implement this method.

  And in terms of the lab orals and assessment there should be a standardised way of marking. Becuase some GTAs give different information to others. For example one GTA told me and others that in the DFT lab that the bar graph is only valid if symmetrically from the middle, while the GTA giving me the oral assessment told me that is only correct when the left had side of the symmetry is removed. This led to me losing marks in the oral assessment